This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-2. (previously canceled)

3. (currently amended): A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region for each of first and second transistors;

forming off-set spacers along side-walls of the gate electrode of each of the first and second transistors;

after forming said off-set spacers, performing a DDD implant to form DDD source and DDD drain regions in the body region for the first transistor;

after said DDD implant, forming main spacers adjacent the off-set spacers of at least the ~~second~~ first transistor;

~~after forming said main spacers,~~ performing a LDD implant to form LDD source and LDD drain regions for the second transistor; and

after forming the main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and DDD source regions and each of the LDD drain and LDD source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

4. (currently amended): The method of claim 3 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions is inversely dependent on a thickness of the off-set spacers,

~~the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off set spacer only;~~ and

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the corresponding highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers.

5. (currently amended): A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region for each of first and second transistors;

forming off-set spacers along side-walls of the gate electrode of each of the first and second transistors;

after forming said off-set spacers, performing a DDD implant to form DDD source and DDD drain regions in the body region for the first transistor;

after forming said off-set spacers, performing a LDD implant to form LDD source and LDD drain regions for the second transistor;

after both said DDD and LDD implants, forming main spacers adjacent the off-set spacers of the first and second transistors; and

after forming said main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and DDD source regions and each of the LDD drain and LDD source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

6. (currently amended): The method of claim 5 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions, and the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the corresponding highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the corresponding highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

7. (original): The method of claim 5 wherein N- type impurities is used in each of the DDD and LDD implants, and N+ type impurities is used in the S/D implant.

8. (original): The method of claim 5 wherein P- type impurities is used in each of the DDD and LDD implants, and P+ type impurities is used in the S/D implant.

9. (currently amended): A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region for each of first and second transistors;

performing a DDD implant to from DDD source and DDD drain regions in the body region for the first transistor;

after said DDD implant, forming off-set spacers along side-walls of the gate electrode of each of the first and second transistors; ~~and~~

after forming said off-set spacers, performing a LDD implant to from LDD source and LDD drain regions in the body region for the second transistor;

after said LDD implant, forming main spacers adjacent the off-set spacers of at least the second transistor; and

after forming the main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and source regions and the LDD drain and source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

10. (currently canceled)

11. (currently amended): The method of claim ~~10~~ 9 wherein,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

~~a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only,~~ and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the corresponding highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

12. (previously amended): The method of claim 9 wherein the off-set spacers are from oxide or oxynitride.

13-14. (currently canceled)

15. (previously canceled)

16. (currently canceled)

17. (previously canceled)

18. (currently amended): The method of claim 9 wherein thicker off-set spacers result in smaller overlap between the first gate electrode and each of the LDD source and drain regions of the second transistor.

19-76. (previously canceled)

77-89. (currently canceled)

90-99. (previously canceled)